REMARKS

Claims 1 and 23 have been amended to incorporate therein the recitation of claim 7, to recite that the difference between the growth temperature of the barrier sublayer C and the growth temperature of the barrier sublayer E is 50°C or more. Claim 7 has been canceled. Also, claim 1 has been amended to recite that the barrier sublayer E is grown by maintaining the lowered growth temperature after lowering the temperature. Support is found, for example, at page 9, lines 29-31 of the present specification.

Review and reconsideration on the merits are requested.

In response to the objection, Applicants submit herewith a new Abstract which conforms with USPTO guidelines.

Claims 16 and 17 were rejected under 35 U.S.C. § 112, second paragraph. As to claim 16, the Examiner considered the language "stacked alternately" to be indefinite, because only two layers are defined. The Examiner further rejected claim 17 as being indefinite.

In response, claim 15 (from which claims 16 and 17 depend) has been amended to more clearly recite that a concentration of the n-type dopant in the layer containing the n-type dopant varies periodically. Claim 16 depending from claim 15 has been amended to recite that a layer with a lower concentration of the n-type dopant is an undoped layer, whereas claim 17 has been amended to recite that a layer with a higher concentration of the n-type dopant is not thicker than a layer with a lower concentration of the n-type dopant.

Claims 13 and 14 have been amended to correct informalities noted by the Examiner.

It is respectfully submitted that the amended claims fully comply with 35 U.S.C. § 112, and withdrawal of the foregoing rejection is respectfully requested.

Description of the Invention:

Fig. 1 of the present description is a graph showing a growth temperature profile of a quantum well structure of a nitride semiconductor light-emitting layer of Example 1. The light-emitting layer comprises a well layer (6), a barrier sublayer A (1) whose growth is started at a low temperature after completing growth of a well layer (6), a barrier sublayer B (2) which is grown in a temperature elevation step, a barrier sublayer C (3) which is grown by maintaining the elevated growth temperature, a barrier sublayer D (4) which is grown in a temperature lowering step and a barrier sublayer E (5) which is grown by maintaining the lowered growth temperature after lowering the temperature (see page 9, lines 16-31 of the present specification).

As claimed in claim 1, the barrier layer comprises a barrier sublayer C and a barrier sublayer E. Further, an object of the present invention, which is to provide a nitride semiconductor device which does not suffer time-dependent deterioration in reverse withstand voltage and which maintains a satisfactory initial reverse withstand voltage, is thereby achieved.

Prior to amendment, claim 1 provided that the barrier sublayer E is grown at a temperature lower than a growth temperature of the barrier sublayer C, and therefore the barrier sublayer E included the barrier sublayer D. In amended claim 1, however, the barrier sublayer E does not include the barrier sublayer D. This is because amended claim 1 recites that the barrier sublayer E is grown by maintaining the lowered growth temperature after lowering the temperature.

Response to Rejection over Prior Art:

Claims 1-12, 15-17, 19-21 and 23-29 were rejected under 35 U.S.C. § 102(b) as being anticipated by JP-A-2002-043618 (JP '618). The Examiner considered JP '618 as meeting each of the terms of the rejected claims, including the barrier sublayer E grown at a temperature lower

than that of barrier sublayer C, where barrier sublayer C is disposed closer to the substrate than the barrier sublayer E.

Applicants traverse, and respectfully request the Examiner to reconsider in view of the amendment to the claims and the following remarks.

JP '618 discloses a barrier sublayer B, a barrier sublayer C and a barrier sublayer D in paragraphs [0027], [0029] and [0058], however there is no description or suggestion of a barrier sublayer A (claim 3) and a barrier sublayer E.

Therefore, the light-emitting device disclosed by JP '618 corresponds to that of Comparative Example 1 or Comparative Example 2 of the present specification. Fig. 5 of the present specification is a graph which shows aging test results of the samples of Examples 1 and 2, and Fig. 6 is a graph which shows aging test results of the samples of Comparative Examples 1 and 2. As clearly seen from a comparison between Fig. 5 and Fig. 6, the light-emitting device of the present invention (i.e., those of Examples 1 and 2) exhibits superior time-dependent deterioration in reverse withstand voltage than that of JP '618 (i.e., Comparative Examples 1 and 2).

Present claim 23 recites "growing a barrier layer of the quantum well structure at the elevated temperature, which is higher than a growth temperature of the well layer; subsequently, lowering the growth temperature; and further growing the barrier layer at the lowered temperature", which original limitation distinguishes barrier sublayer E from barrier sublayer D. Therefore, novelty and inventive step of claim 23 were approved in the International Search Report (ISR) which correctly recognized that JP '618 discloses barrier sublayer D but does not disclose growing barrier sublayer E. To further distinguish over JP '618, claim 23 was amended to recite growing a barrier layer of the quantum well structure at an elevated temperature which

is higher than a growth temperature of the well layer by 50°C or more, subsequently lowering the growth temperature again by 50°C or more, and further growing the barrier layer at the lower temperature.

A partial English translation of JP '618 is attached hereto for the Examiner's reference.

For the above reasons, it is respectfully submitted that the amended claims define novel subject matter, and withdrawal of the foregoing rejection under 35 U.S.C. § 102(b) is respectfully requested.

Claims 13, 14 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over JP '618.

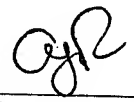
Applicants rely on the response above with respect to the rejection of claims 1-12, 15-17, 19-21 and 23-29 over JP '618.

Withdrawal of all rejections and allowance of claims 1-6 and 8-30 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Partial English Translation of JP'618

[0027]

[Embodiment of the Invention] The invention described in claim 1 is a production method of a nitride semiconductor product having a multiple quantum well structure, in which a well layer composed of a nitride semiconductor and a barrier layer composed of a nitride semiconductor having a larger bandgap energy than that of the nitride semiconductor forming the well layer are stacked alternately, on a substrate, wherein the multiple quantum well structure is formed by repeating the following steps in this order:

a first step growing said well layer at the first substrate temperature;

a second step growing said barrier layer while elevating a temperature toward the second substrate temperature higher than said first substrate temperature from said first substrate temperature; and

a third step lowering a temperature from said second substrate temperature to said first substrate temperature.

[0029] The invention described in claim 2 is a production method of a nitride semiconductor product according to claim 1, wherein there is prepared a fourth step in which said barrier layer is further grown at the substrate temperature which maintained said second substrate temperature at almost constant, after growing said barrier layer by said second step before said third step. Since a part of barrier layer is grown in the condition of maintaining the substrate temperature higher than the

substrate temperature at which a well layer is grown, the crystallinity of a barrier layer can be raised further.

[0058] After the barrier layer is grown at substrate temperature higher than the substrate temperature at which a well layer is grown, when the substrate temperature is lowered to the temperature at which a well layer is grown, it is desirable to grow a part of barrier layer, from a standpoint of shortening the growth time. At the time of lowering the temperature, since the influence on a well layer (crystalline degradation) decreases as compared with the time of elevating the temperature after growing a well layer, there is an advantage that a growth rate can be made fast as compared with said time of elevating the temperature. In addition, since it is clear that a barrier layer grown at an elevated temperature has a good crystallinity, a growth rate at the initial time of lowering the temperature is made fast and the growth rate can be made slow gradually with a drop of the temperature. Thereby, the growth time of MQW is shortened, and the manufacturing cost of a nitride semiconductor product which comprises a MQW light-emitting layer is reduced.